IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 13, 17, 21, 26 and 28-30 AMEND claims 11, 15, 19, 23 and 27 in accordance with the following:

1-10 (CANCELLED)

11. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction in a current processing stage, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal as a through instruction upon determining at least the kind of instruction;

a first processing unit ~~that~~ provided in the current processing stage and connected to the first instruction decoding unit, the first processing unit being configured to ~~performs~~ perform a first operation on a first data when receiving the first control signal, and ~~passes~~ to pass through the first data when receiving the second control signal;

a latch circuit provided between the current processing stage and a next processing stage, the latch circuit holding one of a result of the first operation and the first data passing through the first processing unit as a second data;

a second instruction decoding unit that determines at least a kind of instruction in a next processing stage, decodes a second instruction into a third control signal, and decodes all other instructions with the exception of the second instruction into a fourth control signal upon determining at least the kind of instruction;

a second processing unit ~~that~~ provided in the next processing stage and connected to the second instruction decoding unit, the second processing unit being configured to perform ~~performs~~ a second operation on ~~a~~ the second data when receiving the third control signal~~, the second data being an output of the first processing unit~~; and

a multiplexer provided in the next processing stage for selecting ~~that selects~~ an output of the second processing unit or the second data held in the latch circuit based on an output of the

second instruction decoding unit~~, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage~~.

12. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 11, wherein

the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal.

13. (CANCELLED)

14. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 11, wherein the first processing unit receives multiple data as the first data.

15. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first latch circuit provided in a current processing stage for storing a first data;

a first instruction decoding unit that determines at least a kind of instruction in the current processing stage, that decodes a first instruction into a first control signal, and that decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction;

a first processing unit provided in the current processing stage and connected to the first instruction decoding unit, the first processing unit being configured to perform ~~that performs~~ a first operation on a first data when receiving the first control signal;

a bypass line provided in parallel with the first processing unit;

a multiplexer provided in the current processing stage for selecting one of ~~that selects~~ an output of the first processing unit or the first data held in the first latch circuit based on an output of the first instruction decoding unit;

a second latch circuit provided between the current processing stage and a next processing stage, the second latch circuit holding one of a result of the first operation and the first data bypassing the first processing unit through the bypass line as a second data;

a second instruction decoding unit that determines at least a kind of instruction in the next processing stage, that decodes a second instruction into a third control signal, and that decodes all other instructions with the exception of the second instruction into a fourth control

signal as a through instruction upon determining at least the kind of instruction; and

a second processing unit provided in the next processing stage and connected to the second instruction decoding unit, the second processing unit being configured to perform ~~that performs~~ a second operation on ~~a~~ the second data when receiving the third control signal, and ~~passes~~ to pass the second data when receiving the fourth control signal~~, where the second data is an output of the multiplexer~~.

16. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 15, wherein

the multiplexer selects an output of the first processing unit when receiving the first control signal, and selects the first data when receiving the second control signal.

17. (CANCELLED)

18. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 15, wherein

the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data.

19. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction in a current processing stage, that decodes a first instruction into a first control signal, and that decodes all other instructions with the exception of the first instruction into a second control signal as a through instruction upon determining at least the kind of instruction;

a first processing unit provided in the current processing stage and connected to the first instruction decoding unit, the first processing unit being configured to ~~that performs~~ perform a first operation on a first data when receiving the first control signal, and ~~passes~~ to pass the first data when receiving the second control signal;

a latch circuit provided between the current processing stage and a next processing stage, the latch circuit holding one of a result of the first operation and the first data passing through the first processing unit as a second data;

a second instruction decoding unit that determines at least a kind of instruction in the next processing stage, that decodes the first instruction into a third control signal, decodes a

second instruction into a fourth control signal, and decodes all other instructions with the exception of the first and second instructions into a fifth control signal upon determining at least the kind of instruction;

a second processing unit provided in the next processing stage and connected to the second instruction decoding unit, the second processing unit being configured to perform ~~that performs~~ a second operation on a second data when receiving the third control signal, and performs a third operation on the second data when receiving the fourth control signal~~, where the second data is an output of the first processing unit~~; and

a multiplexer provided in the next processing stage for selecting ~~that selects~~ an output of the second processing unit or the second data held in the latch circuit based on an output of the second instruction decoding unit~~, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage~~.

20. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 19, wherein

the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal.

21. (CANCELLED)

22. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 19, wherein the first processing unit receives multiple data as the first data.

23. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first latch circuit provided in a current processing stage for storing a first data;

a first instruction decoding unit that determines at least a kind of instruction in the current processing stage, that decodes a first instruction into a first control signal, decodes a second instruction into a second control signal, and decodes all other instructions with the exception of the first and second instructions into a third control signal upon determining at least the kind of instruction;

a first processing unit ~~that performs~~ provided in the current processing stage and

connected to the first instruction decoding unit, the first processing unit being configured to perform a first operation on a first data when receiving the first control signal, and performs a second operation on the first data when receiving the second control signal;

a bypass line provided in parallel with the first processing unit;

a multiplexer ~~that selects~~ provided in the current processing stage for selecting one of an output of the first processing unit or the first data held in the first latch circuit based on an output of the first instruction decoding unit;

a second latch circuit provided between the current processing stage and a next processing stage, the second latch circuit holding one of a result of the first operation and the first data bypassing the first processing unit through the bypass line as a second data;

a second instruction decoding unit provided in the next processing stage, that decodes the first instruction into a fourth control signal, and that decodes all other instructions with the exception of the first instruction into a fifth control signal as a through instruction upon determining at least the kind of instruction; and

a second processing unit ~~that performs~~ provided in the next processing stage and connected to the second instruction decoding unit, the second processing unit being configured to perform a third operation on a second data when receiving the fourth control signal, and ~~passes~~ to pass the second data when receiving the fifth control signal~~, where the second data is an output of the multiplexer, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage~~.

24. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 23, wherein

the multiplexer selects an output of the first processing unit when receiving either one of the first or the second control signals, and selects the first data when receiving the third control signal.

25. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 23, further comprising:

a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit.

26. (CANCELLED)

27. (CURRENTLY AMENDED) A processor execution pipeline having at least a latching unit to hold and output data, comprising:

a first instruction decoding unit to convert a first instruction into a first control signal in a current processing stage, and to convert all other instructions with the exception of the first instruction into a second control signal as a through instruction;

a first processing unit provided in the current processing stage and connected to the first instruction decoding unit, the first processing unit being configured to perform a first operation on a first data when receiving the first control signal, and to pass the first data when receiving the second control signal;

a latching circuit provided between the current processing stage and a next processing stage, the latch circuit holding one of a result of the first operation and the first data passing the first processing unit as a second data;

a second instruction decoding unit in the next processing stage to convert a second instruction into a third control signal, and to convert all other instructions with the exception of the second instruction into a fourth control signal;

a second processing unit provided in the next processing stage and connected to the second instruction decoding unit, the second processing unit being configured to perform a second operation on ~~a~~ the second data when receiving the third control signal ~~where the second data is an output of the first processing unit~~; and

a multiplexer provided in the next processing stage for selecting ~~that selects~~ an output of the second processing unit or the second data held in the latching circuit based on an output of the second instruction decoding unit;

wherein the latching unit is configured ~~holds an output of the first processing unit and the second data is held by the latching unit allowing the latching unit~~ to be shared by the first processing unit and the second processing ~~units~~unit~~, and the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage~~.

28-30. (CANCELLED)